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DEEP WELL IMPLANT STRUCTURE PROVIDING LATCH-UP RESISTANT CMOS SEMICONDUCTOR PRODUCT

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The invention relates generally to CMOS semiconductor products. More particularly, the invention relates to latch-up resistant CMOS semiconductor products.

2. Description of the Related Art

[0002] Semiconductor products are fabricated employing transistors as switching elements within circuits typically directed to either data storage applications or data manipulation applications. Particularly common semiconductor products are complementary metal oxide semiconductor (CMOS) semiconductor products. CMOS products employ alternating arrays of n-channel metal oxide semiconductor (MOS) transistors and p-channel metal oxide semiconductor (MOS) transistors. CMOS semiconductor products are generally desirable since they are easy to fabricate and they operate efficiently.

[0003] Although CMOS semiconductor products are quite common, they are nonetheless not entirely without problems. In particular, due to the presence of complementary polarities of MOS transistors, CMOS semiconductor products are often susceptible to latch-up. Latch-up is a phenomenon where various doped components within opposite polarity MOS transistors electrically connect to form undesirable parasitic devices, such

as parasitic transistors. Latch-up effects become pronounced as CMOS semiconductor product dimensions decrease. They often provide electrical current flows that may physically damage CMOS semiconductor products.

[0004] Desirable are latch-up resistant CMOS semiconductor products that may be readily fabricated.

[0005] The invention is directed towards the foregoing object.

SUMMARY OF THE INVENTION

[0006] A first object of the invention is to provide a CMOS semiconductor product.

[0007] A second object of the invention is to provide a CMOS semiconductor product in accord with the first object of the invention, where the CMOS semiconductor product is resistant to latch-up.

[0008] In accord with the objects of the invention, the invention provides a CMOS semiconductor product and a method for operating the CMOS semiconductor product.

[0009] The CMOS semiconductor product comprises a semiconductor substrate. A first doped well of a first polarity and a laterally separated second doped well of a second polarity opposite the first polarity are both formed into the

semiconductor substrate. A third doped well of the second polarity is formed laterally and vertically surrounding the first doped well of the first polarity. Finally, a MOS transistor of the second polarity is formed within and upon the first doped well and a MOS transistor of the first polarity is formed within and upon the second doped well.

[0010] The invention provides a latch-up resistant CMOS semiconductor product that may be readily fabricated.

[0011] The invention realizes the foregoing object by employing a third doped well of a second polarity laterally and vertically surrounding a first doped well of a first polarity within a semiconductor substrate. A second doped well of the second polarity is also formed within the semiconductor substrate and laterally separated from the first doped well of the first polarity. A MOS transistor of the first polarity is formed within the second doped well and a MOS transistor of the second polarity is formed within the first doped well. Under typical operating conditions for the CMOS semiconductor product, the third doped well reduces a susceptibility to a snap-back phenomenon when operating the CMOS semiconductor product. Thus, latch-up susceptibility is also reduced within the CMOS semiconductor product.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The objects, features and advantages of the invention are understood within the context of the Description of the

Preferred Embodiment, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

[0013] Fig. 1, Fig. 2, Fig. 3, Fig. 4 and Fig. 5 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in fabricating a CMOS semiconductor product in accord with a preferred embodiment of the invention.

[0014] Fig. 6 shows a graph of Current Density versus Threshold Voltage for CMOS semiconductor products fabricated in accord and not in accord with the invention.

[0015] Fig. 7 shows an additional graph of Current Density versus Threshold Voltage for a CMOS semiconductor product fabricated in accord with the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0016] The invention provides a CMOS semiconductor product that may be readily fabricated with reduced susceptibility to latch-up.

[0017] The invention realizes the foregoing object by employing a third doped well of a second polarity laterally and vertically surrounding a first doped well of a first polarity within a semiconductor substrate. A second doped well of the

second polarity is also formed within the semiconductor substrate and laterally separated from the first doped well of the first polarity. A MOS transistor of the first polarity is formed within the second doped well and a MOS transistor of the second polarity is formed within the first doped well. Under typical operating conditions for the CMOS semiconductor product, the third doped well reduces susceptibility to a snap-back phenomenon when operating the CMOS semiconductor product. Thus, latch-up susceptibility is also reduced within the CMOS semiconductor product.

[0018] The preferred embodiment illustrates the invention within the context of a CMOS product fabricated employing a p polarity substrate having formed therein a p well laterally separated from an n well, and where the p well is further embedded within a deeper n well that laterally and vertically further isolates the p well from the n well. However, the invention is not intended to be so limited. Rather the invention may be practiced with a semiconductor substrate of either p polarity or n polarity. The invention may also be practiced employing an alternate complementary configuration of an n well embedded within a deeper p well such as to provide a CMOS semiconductor product with latch-up resistance.

[0019] Fig. 1 to Fig. 5 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in fabricating a CMOS semiconductor product in accord with the invention.

[0020] Fig. 1 shows a semiconductor substrate 10. A pair of initial doped wells 12a and 12b is formed laterally separated within the semiconductor substrate 10. The pair of initial doped wells 12a and 12b may be laterally (i.e., horizontally) separated by a separation distance W1 of much less than about 15 microns and preferably in a range of from about 5 to about 10 microns. The semiconductor substrate 10 is preferably a p polarity semiconductor substrate, but as disclosed above an n polarity semiconductor substrate may also be employed. Each of the pair of initial doped wells 12a and 12b is preferably an n doped well. The semiconductor substrate 10 preferably has a p dopant concentration of from about 1E8 to about 1E10 dopant atoms per cubic centimeter. Each of the initial doped wells 12a and 12b preferably has an n dopant concentration of from about 1E11 to about 1E12 dopant atoms per cubic centimeter. The initial doped well 12b is intended to correspond with a second doped well in accord with the invention as broadly claimed.

[0021] Fig. 2 shows the results of forming an additional doped well 14 within the initial doped well 12a, thus providing a pair of separated initial doped wells 12a' and 12a" adjoining but not beneath the additional doped well 14. Each of the separated initial doped wells 12a' and 12a'' has a linewidth W2 of from about 0.5 to about 1.0 microns. The additional doped well 14 is formed of a p polarity opposite the n polarity of the initial doped wells 12a and 12b, and of the same p polarity as the substrate 10. The additional doped well 14 is formed of a p dopant concentration from about 1E13 to about 1E14. The additional doped well 14 is intended to correspond with a first

doped well in accord with the invention as broadly claimed. The separated initial doped well 12a", which still has an n dopant concentration of from about 1E11 to about 1E12 dopant atoms per cubic centimeter, is intended to correspond with a fourth doped well in accord with the invention as broadly claimed.

[0022] Fig. 3 shows a further additional doped well 16 formed such that the additional doped well 14 is embedded into the further additional doped well 16 while being laterally (i.e., horizontally) and vertically surrounded by the further additional doped well 16. The further additional doped well 16 thus completely isolates the additional doped well 14 from the initial doped well 12b. The further additional doped well 16 is formed to a depth D1 beneath additional doped well 14 of from about 1000 to about 10000 angstroms and a linewidth W3 adjoining the further doped well 14 of from about 0.2 to about 0.5 microns. The further additional doped well 16 is of n polarity. The further additional doped well 16 is formed with a dopant concentration of from about 1E11 to about 1E12 dopant atoms per cubic centimeter, as is the pair of initial doped wells 12a and 12b. The further additional doped well 16 is intended to correspond with a third doped well in accord with the invention as broadly claimed.

[0023] Fig. 4 shows a series of first doped connections 18a, 18b, 18c and 18d within the additional doped well 14, the separated intital doped well 12a" and the initial doped well 12b. The first doped connections 18a, 18b, 18c and 18d are of n polarity. The first doped connections 18a and 18b are intended

as source/drain regions. The first doped connections 18c and 18d are intended as ohmic connections to the n well regions into which they are formed. Fig. 4 also shows a series of second doped connections 20a, 20b, 20c and 20d. The series of second doped connections 20a, 20b, 20c and 20d is formed of p polarity. The second doped connections 20a and 20b are intended as ohmic connections within the p substrate 10 or p additional doped well 14 within which they are formed. The second doped connections 20c and 20d are intended as source/drain regions. Each of the series of first doped connections 18a, 18b, 18c and 18d and the series of second doped connections 20a, 20b, 20c and 20d is formed of a dopant concentration from about 1E18 to about 1E20 dopant atoms per cubic centimeter.

[0024] Finally, Fig. 4 also shows a pair of gate electrodes 22a and 22b. Corresponding gate dielectric layers are omitted for clarity. The pair of first doped connections 18a and 18b of n polarity form an n MOS transistor in conjunction with the gate electrode 22a. The pair of second doped connections 20a and 20b of p polarity form a p MOS transistor in conjunction with the gate electrode 22b. The n MOS transistor and the p MOS transistor provide a CMOS semiconductor product fabricated within the semiconductor substrate 10.

[0025] Fig. 5 shows various connections and interconnections to the doped connections 18a, 18b, 18c, 18d, 20a, 20b, 20c and 20d within the CMOS semiconductor product of Fig. 4. The doped connections 20a and 20b, as well as the doped connection 18a that serves as a source/drain region within the n MOS

transistor, are all connected to Vss as ground. Source/drain regions 18b and 20d are connected together. Doped connections 18c and 18d, and source/drain region 20c are connected in common as Vcc such as to energize the CMOS semiconductor product.

[0026] Within the CMOS semiconductor product as illustrated in Fig. 5, no guard ring structures are employed surrounding either of the MOS transistors. In addition, incident to energizing the CMOS semiconductor product as illustrated in accord with Fig. 5, no parasitic transistor is formed between the first MOS transistor and the second MOS transistor since the Vcc voltage is the same at the separated initial doped well 12a" and the further additional doped well 16, with respect to the initial doped well 12b. Since no parasitic transistor is formed the invention allows for a reduction of separation distance of the initial doped well 12b and the separated initial doped well 12a" which in turn provides for a reduced separation distance of the pair of MOS transistors. The specific ordering for forming the doped wells that provide the CMOS semiconductor product of Fig. 5 is not limited to the sequence illustrated in Figs. 1-4, but rather alternative orderings may also be employed.

Examples

[0027] In order to illustrate the value of the invention, a CMOS semiconductor product was fabricated in accord with Fig. 5. An additional CMOS semiconductor product was also fabricated, but absent the further additional doped well 16.

[0028] Current density versus threshold voltage measurements were obtained for each of the CMOS semiconductor products at a Vdd voltage of 1.0 volts. Results of the measurements are illustrated in the graph of Fig. 6. Within Fig. 6, reference numeral 60 corresponds with electrical data points obtained for the CMOS semiconductor product in accord with the invention. Reference numeral 62 corresponds with electrical data points obtained for the CMOS semiconductor product absent the further additional doped well 16. The data points corresponding with reference numeral 62 illustrate a pair of dislocations 62a and 62b that are indicative of a voltage snap-back phenomenon. The voltage snap-back phenomenon is in turn indicative of CMOS semiconductor product latch-up.

[0029] Fig. 7 shows an additional measurement of a CMOS semiconductor product in accord with the invention undertaken at a Vdd of 2.5 volts rather than 1.0 volts. As is illustrated in Fig. 7, even at an increased Vdd of 2.5 volts a CMOS semiconductor product fabricated in accord with the invention does not show a snap-back or latch-up effect.

[0030] The preferred embodiment and examples of the invention are illustrative of the invention rather than limiting of the invention. Revisions and modifications may be made to materials, structures and dimensions of a semiconductor product in accord with the preferred embodiment and examples of the invention while still providing a semiconductor product in accord with the invention, further in accord with the accompanying claims.